SPECIFICATION AMENDMENTS

At page 1, lines 1-2, please amend the Title as follows:

~~MICROPROCESSOR WITH HARDWARE CONTROLLED POWER MANAGEMENT~~ SIGNAL-INITIATED POWER MANAGEMENT METHOD FOR A PIPELINED DATA PROCESSOR

At page 1, between lines 2 and 3, please insert the following:

RELATED APPLICATIONS

This is a division of U.S. patent application no. 10/216,615, filed August 9, 2002.

At page 1, lines 4-6, please amend the text of the section entitled "Technical Field of the Invention" as follows:

This invention relates in general to integrated circuits, and more particularly to a ~~microprocessor having hardware controlled~~ pipelined data processor with power management control.

At page 4, lines 3-21, please amend the text of the section entitled "Summary of the Invention" as follows:

~~In accordance with the present invention, a method and apparatus is provided which provides significant advantages in reducing the power consumption of a microprocessor.~~

~~In the present invention, a processing unit includes a plurality of subcircuits and circuitry for generating a clock signal thereto. Circuitry is provided for detecting the assertion of a control signal; responsive to the control signal, disabling circuitry disables the clock signal to one or more of the subcircuits.~~

~~The present invention provides significant advantages over the prior art. A significant reduction in the power consumed by a computer may be effected by disabling the clock to the microprocessor circuitry. The present invention allows the disabling and enabling of the microprocessor clock signals to be controlled by a single control signal. Further, an acknowledge signal may be provided to notify external circuitry of the suspended state of the microprocessor.~~

In accordance with the presently claimed invention, a signal-initiated power management method for a pipelined data processor is provided by which a clock signal to pipeline subcircuitry is selectively disabled in response to at least one control signal.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination;

generating, in response to the at least one clock control signal, at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively; and

selectively operating, in response to the first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one

or more incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states;

generating, in response to the at least one clock control signal, at least a first clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination; and

selectively operating, in response to the first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination;

generating, in response to the at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively; and

selectively operating, in response to the first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of the plurality of first clock signal cycles, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to at least a second one subsequent to the first one of the plurality of first clock signal cycles, the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states;

generating, in response to the at least one clock control signal, at least a first clock signal having an active state having a plurality of successive cycles and an

inactive state having substantially zero cycles corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the inactive state following the first incoming control signal states combination; and

selectively operating, in response to the first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of the plurality of first clock signal cycles, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to at least a second one subsequent to the first one of the plurality of first clock signal cycles, the one or more decoded instructions.

In accordance with another embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states with the respective assertion states following the first incoming control signal states combination;

generating, in response to the at least one clock control signal, the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively; and

executing, with at least a portion of a plurality of subcircuits including

pipeline subcircuitry in response to the active second clock signal, one or more instructions for data processing.

In accordance with another embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to the one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to the one or more incoming control signal assertion and de-assertion states;

generating, in response to the at least one clock control signal, the first clock signal having active and inactive states substantially independent of the at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to the at least one clock control signal de-assertion and assertion states, respectively, with the second clock signal inactive state following the first incoming control signal states combination; and

executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to the active second clock signal, one or more instructions for data processing.

At page 19, lines 3-8, please amend the text of the section entitled "Abstract of the Disclosure" as follows:

~~A processing unit includes a plurality of subcircuits and circuitry for generating clock signals thereto. Detection circuitry detects the assertion of a control signal and disabling circuitry is operable to disable the clock signals to one or more of the subcircuits responsive to the control signal.~~ A signal-initiated power management method for a pipelined data processor by which a clock signal to pipeline subcircuitry

is selectively disabled in response to at least one control signal.